

3 BAND CAR AUDIO PROCESSOR

1 FEATURES

- 4 STEREO INPUTS
- SOFT STEP VOLUME
- BASS, MIDDLE, TREBLE AND LOUDNESS
- DIRECT MUTE AND SOFTMUTE
- FOUR INDEPENDENT SPEAKER OUTPUTS
- SUB WOOFER OUTPUT
- SOFT STEP SPEAKER/SUBWOOFER CONTROL
- 7 BANDS SPECTRUM ANALYZER
- DIGITAL CONTROL:
 - I²C-BUS INTERFACE

2 DESCRIPTION

The TDA7419 is a high performance signal processor specifically designed for car radio applications. The device includes a high performance audiopro-

Figure 2. Block Diagram

Figure 1. Package

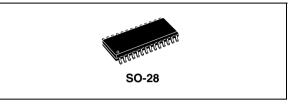
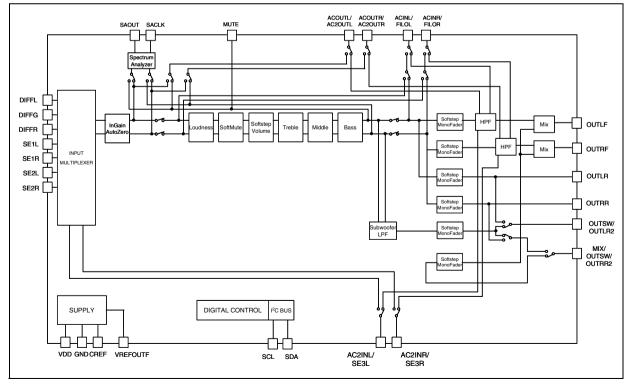


Table 1. Order Codes

Part Number	Package
TDA7419	SO-28
TDA7419TR	SO-28 in Tape & Reel

cessor with fully integrated audio filters. The digital control allows programming in a wide range of filter characteristics. By the use of BICMOS-process and linear signal processing low distortion and low noise are obtained.



March 2005

Table 2. Supply

Symbol	Parameter	Test Condition	Min.	Тур.	Max.	Unit
Vs	Supply Voltage		7.5	8.5	10.5	V
ls	Supply Current	V _s = 8.5V	30	35	40	mA
SVRR	Ripple Rejection @ 1KHz	Audioprocessor(all Filters flat)	60			dB

Table 3. Thermal Data

Symbol	Parameter	Value	Unit
R _{Th j} -pins	Thermal Resistance Junction-pins max	85	°C/W

Table 4. Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
Vs	Operating Supply Voltage	10.5	V
T _{amb}	Operating Temperature Range	-40 to 85	°C
T _{stg}	Storage Temperature Range	-55 to +150	°C

ESD

All pins are protected against ESD according to the MIL883 standard.

Figure 3. Pin connection (Top view)

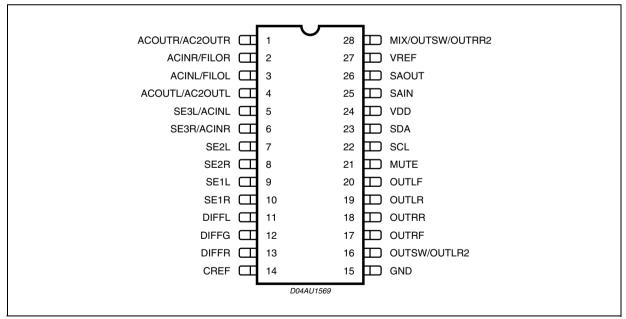


Table 5. Pin Description

Pin N#	Pin Name	Function	I/O
1	ACOUTR / AC2OUTR	AC coupling right output / DSO filter AC2OUT right channel	0
2	ACINR / FILOR	AC coupling right input / DSO filter FILO right channel	I/O
3	ACINL / FILOL	AC coupling left input / DSO filter FILO left channel	I/O
4	ACOUTL / AC2OUTL	AC coupling left output / DSO filter AC2OUT left channel	0
5	SE3L / ACINL	Single-ended input 3 left channel / AC coupling left input	I
6	SE3R / ACINR	Single-ended input 3 right channel / AC coupling right input	I
7	SE2L	Single-ended input 2 left channel	I
8	SE2R	Single-ended input 2 right channel	I
9	SE1L	Single-ended input 1 left channel	I
10	SE1R	Single-ended input 1 Right channel	I
11	DIFFL	Pseudo differential stereo input left	I
12	DIFFG	Pseudo differential stereo input common	1
13	DIFFR Pseudo differential stereo input right		I
14	CREF	Reference capacitor	0
15	GND	Ground	S
16	OUTSW / OUTLR2	Subwoofer output / 2 nd rear left output	0
17	OUTRF	Front right output	0
18	OUTRR	Rear right output	0
19	OUTLR	Rear left output	0
20	OUTLF	Front left output	0
21	MUTE	External mute pin	I
22	SCL	I2C bus clock	I
23	SDA	I2C bus data	I/O
24	VDD	Supply	S
25	SAIN	Spectrum analyzer clock input	I
26	SAOUT	Spectrum analyzer output	0
27	VREF	Vref output	0
28	MIX / OUTSW / OUTRR2	Mix input / Additional subwoofer output / 2 nd rear right output	I/O

3 Audio Processor Features:

Input Multiplexer	QD / SE: quasi-differential stereo inputs, with selectable single-ended mode SE1: stereo single-ended input SE2: stereo single-ended input SE3 / AC2IN: stereo single-ended input / DSO filter input In-Gain 0 to 15dB, 1dB steps internal offset-cancellation (AutoZero) separate second source-selector
Mixing stage	mixable to front speaker-outputs
Loudness	2nd order frequency response programmable center frequency (400Hz/800Hz/2400Hz) 15dB with 1dB steps selectable low & high frequency boost selectable flat-mode (constant attenuation)
Volume	+15dB to -79dB with 1dB step resolution soft-step control with programmable blend times
Bass	2nd order frequency response center frequency programmable in 4 steps (60Hz/80Hz/100Hz/200Hz) Q programmable 1.0/1.25/1.5/2.0 DC gain programmable -15 to 15dB range with 1dB resolution
Middle	2nd order frequency response center frequency programmable in 4 steps (500Hz/1KHz/1.5KHz/2.5KHz) Q programmable 0.5/0.75/1.0/1.25 DC gain programmable -15 to 15dB range with 1dB resolution
Treble	2nd order frequency response center frequency programmable in 4 steps (10KHz/12.5KHz/15KHz/17.5KHz) -15 to 15dB range with 1dB resolution
Spectrum analyzer	seven bandpass filters 2nd order frequency response programmable Q factor for different visual appearance analog output controlled by external serial clock
Speaker	4 independent soft step speaker controls, +15dB to -79dB with 1dB steps Independent programmable mix input with 50% mixing ratio for front speakers direct mute
Subwoofer	2nd order low pass filter with programmable cut off frequency single-ended mono output independent soft step level control, +15dB to -79dB with 1dB steps
Mute Functions	direct mute digitally controlled SoftMute with 3 programmable mute-times(0.48ms/0.96ms/ 123ms)
Effect	gain effect, or high pass effect with fixed external components

4 ELECTRICAL CHARACTERISTICS

Table 6. Electrical Characteristcs

 $V_S = 8.5V$; $T_{amb} = 25^{\circ}C$; $R_L = 10k\Omega$; all gains = 0dB; f = 1kHz; unless otherwise specified

Symbol	Parameter	Test Condition	Min.	Тур.	Max.	Unit
SUPPLY	•	•	•	•	•	
Vs	Supply Voltage		8	8.5	10	V
ls	Supply Current		27	37	47	mA
INPUT SE	LECTOR					
R _{in}	Input Resistance	All single ended inputs	70	100	130	kΩ
V _{CL}	Clipping level	All Input	1.8	2		V _{RMS}
		QD input	1.7	2		V _{RMS}
S _{IN}	Input Separation		80	100		dB
GIN MIN	Min. Input Gain		-1	0	1	dB
GIN MAX	Max. Input Gain		13	15	17	dB
G _{STEP}	Step Resolution		0.5	1	1.5	dB
V _{DC}	DC Steps	Adjacent Gain Steps	-5	1	5	mV
		G _{MIN} to G _{MAX}	-20	4	20	mV
Voffset	Remaining offset with AutoZero			0.5		mV
DIFFERE	NTIAL STEREO INPUTS					
R _{in}	Input Resistance	Differential	70	100	130	KΩ
CMRR	Common Mode Rejection Ratio	V _{CM} =1 VRMS@ 1kHz	46	70		dB
		V _{CM} =1 VRMS@ 10kHz	46	60		dB
e _{No}	Output Noise @ Speaker Outputs	20Hz-20kHz,flat;all stages 0dB		12		μV
MIXING C	ONTROL					
M_{LEVEL}	Mixing Ratio	Main / Mix Source		-6/-6		dB
G _{MAX}	Max Gain		13	15	17	dB
A _{MAX}	Max Attenuation		-83	-79	-75	dB
A _{STEP}	Step Resolution		0.5	1	1.5	dB
LOUDNE	SS CONTROL		•		•	
A _{MAX}	Max Attenuation		-17	-15	-13	dB
A _{STEP}	Step Resolution		0.5	1	1.5	dB
f _{Peak}	Peak Frequency	f _{P1}	360	400	440	Hz
		f _{P2}	720	800	880	Hz
		f _{P3}	2200	2400	2600	Hz
VOLUME	CONTROL					
G _{MAX}	Max Gain		13	15	17	dB
A _{MAX}	Max Attenuation		-83	-79	-75	dB
ASTEP	Step Resolution		0.5	1	1.5	dB
EA	Attenuation Set Error	G = -20 to +20dB	-0.75	0	+0.75	dB
-4		G = -79 to -20dB	-4	0	3	dB
ET	Tracking Error			-	2	dB
V _{DC}	DC Steps	Adjacent Attenuation Steps	-3	0.1	3	mV
	•	From 0dB to G _{MIN}	-5	0.5	5	mV

Table 6. Electrical Characteristcs (continued)

 $V_S = 8.5V$; $T_{amb} = 25^{\circ}C$; $R_L = 10k\Omega$; all gains = 0dB; f = 1kHz; unless otherwise specified

Symbol	Parameter	Test Condition	Min.	Тур.	Max.	Unit
SOFT MU	TE		•	•	•	•
A _{MUTE}	Mute Attenuation		80	100		dB
TD	Delay Time	T1		0.48	1	ms
		T2		0.96	2	ms
		ТЗ	70	123	170	ms
$V_{\text{TH Low}}$	Low Threshold for SM Pin				1	V
V _{TH High}	High Threshold for SM Pin		2.5			V
R _{PU}	Internal pull-up resistor		32	45	58	kΩ
V _{PU}	Internal pull-up Voltage			3.3		V
BASS CC	NTROL			•	•	
Fc	Center Frequency	f _{C1}	54	60	66	Hz
		f _{C2}	72	80	88	Hz
		f _{C3}	90	100	110	Hz
		f _{C4}	180	200	220	Hz
Q _{BASS}	Quality Factor	Q ₁	0.9	1	1.1	
		Q ₂	1.1	1.25	1.4	
		Q ₃	1.3	1.5	1.7	
		Q ₄	1.8	2	2.2	
CRANGE	Control Range		±14	±15	±16	dB
A _{STEP}	Step Resolution		0.5	1	1.5	dB
DC _{GAIN}	Bass-DC-Gain	DC = off	-1	0	+1	dB
		DC = on (shelving filter, use for cut only)		-4.4		dB
MIDDLE	CONTROL			•	•	
CRANGE	Control Range		±14	±15	±16	dB
A _{STEP}	Step Resolution		0.5	1	1.5	dB
fc	Center Frequency	f _{C1}	400	500	600	Hz
		f _{C2}	0.8	1	1.2	kHz
		f _{C3}	1.2	1.5	1.8	kHz
		f _{C4}	2	2.5	3	kHz
QBASS	Quality Factor	Q ₁	0.45	0.5	0.55	
		Q ₂	0.65	0.75	0.85	
		Q ₃	0.9	1	1.1	
		Q ₄	1.1	1.25	1.4	
TREBLE	CONTROL					1
CRANGE	Clipping Level		±14	±15	±16	dB
A _{STEP}	Step Resolution		0.5	1	1.5	dB
fc	Center Frequency	f _{C1}	8	10	12	kHz
		f _{C2}	10	12.5	15	kHz
		f _{C3}	12	15	18	kHz
		f _{C4}	14	17.5	21	kHz



Table 6. Electrical Characteristcs (continued)

 $V_S = 8.5V$; $T_{amb} = 25^{\circ}C$; $R_L = 10k\Omega$; all gains = 0dB; f = 1kHz; unless otherwise specified

Symbol	Parameter	Test Condition	Min.	Тур.	Max.	Unit
SPEAKE	R ATTENUATORS			•	•	
G _{MAX}	Max Gain		14	15	16	dB
A _{MAX}	Max Attenuation		-83	-79	-75	dB
ASTEP	Step Resolution		0.5	1	1.5	dB
A _{MUTE}	Mute Attenuation		80	90		dB
EE	Attenuation Set Error				2	dB
V _{DC}	DC Steps	Adjacent Attenuation Steps	-5	0.1	5	mV
AUDIO O	UTPUTS					
V _{CL}	Clipping level	d = 0.3%	1.8	2		V _{RMS}
ROUT	Output impedance			30	100	Ω
RL	Output Load Resistance		2			kΩ
CL	Output Load Capacitor				10	nF
V _{DC}	DC Voltage Level		3.8	4.0	4.2	V
SUBWO	OFER ATTENUATOR					
G _{MAX}	Max Gain		14	15	16	dB
A _{MAX}	Max Attenuation		-83	-79	-75	dB
A _{STEP}	Step Resolution		0.5	1	1.5	dB
A _{MUTE}	Mute Attenuation		80	90		dB
EE	Attenuation Set Error				2	dB
V _{DC}	DC Steps	Adjacent Attenuation Steps	-5	1	5	mV
SUBWO	DFER LOWPASS					
f _{LP}	Lowpass Corner Frequency	f _{LP1}	72	80	88	Hz
		f _{LP2}	108	120	132	Hz
		f _{LP3}	144	160	176	Hz
HPF EFF	ЕСТ					
G _{MAX}	Max Gain		21	22	23	dB
G _{MIN}	Min Gain		3	4	5	dB
A _{STEP}	Step Resolution		1.5	2	2.5	dB
SPECTR	UM ANALYZER CONTROL					
V _{SAOut}	Output Voltage Range		0		3.3	V
f _{C1}	Center Frequency Band 1		5.5	62	69	Hz
f _{C2}	Center Frequency Band 2		141	157	173	Hz
f _{C3}	Center Frequency Band 3		356	392	436	Hz
f _{C4}	Center Frequency Band 4		0.9	1	1.1	kHz
f _{C5}	Center Frequency Band 5		2.26	2.51	2.76	kHz
f _{C6}	Center Frequency Band 6		5.70	6.34	6.98	kHz
f _{C7}	Center Frequency Band 7		14.4	16	17.6	kHz
Q	Quality Factor	Q1	1.62	1.8	1.98	
		Q2	3.15	3.5	3.85	
fSACIk	Clock Frequency		3		100	kHz
t _{Sadel}	Analog Output Delay Time		2			μS

Table 6. Electrical Characteristcs (continued)

 $V_S = 8.5V$; $T_{amb} = 25^{\circ}C$; $R_L = 10k\Omega$; all gains = 0dB; f = 1kHz; unless otherwise specified

Symbol	Parameter	Test Condition	Min.	Тур.	Max.	Unit
t _{repeat}	Spectrum Analyzer Repeat Time		50			ms
t _{intres}	Internal Reset Time			4.5		ms
GENERA	L	•	•			
e _{NO}	Output Noise	BW=20Hz to 20 kHz all gain = 0dB		12	20	μV
		BW=20Hz to 20 kHz Output muted		6	15	μV
S/N	Signal to Noise Ratio	all gain = 0dB flat; $V_0 = 2V_{RMS}$		100		dB
D Distortion		V _{IN} = 1V _{RMS} ; all stages 0dB		0.01	0.1	%
S _C	Channel Separation left/right		80	90		dB

5 DESCRIPTION OF THE AUDIOPROCESSOR

5.1 Input stages

In the basic configuration, one stereo quasi-differential and three (two in case of DSO applications) single ended stereo inputs are available.

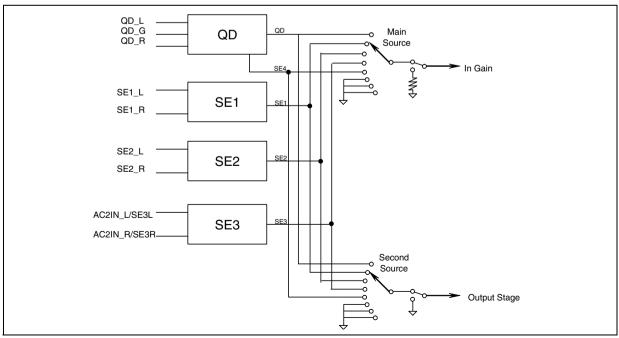
5.1.1 Quasi-differential stereo Input (QD)

The QD input is implemented as a buffered quasi-differential stereo stage with 100k input-impedance at each input. The attenuation is fixed to -3dB in order to adapt the incoming signal level.

5.1.2 Single-ended stereo input (SE1, SE2, SE3/AC2IN)

The input-impedance at each input is 100k and the attenuation is fixed to -3dB for incoming signals. The input for SE3 is also configurable as part of the interface for external filters in DSO applications (AC2IN)

Figure 4. Input Stage



47/

5.2 AutoZero

The AutoZero allows a reduction of the number of pins as well as external components by canceling any offset generated by or before the In-Gain-stage (Please notice that externally generated offsets, e.g. generated through the leakage current of the coupling capacitors, are not canceled).

The auto-zeroing is started every time the input source is changed and needs max. 0.3ms for the alignment. To avoid audible clicks the Audio processor is muted before the loudness stage during this time. The AutoZero feature is only present in the main signal-path.

5.2.1 AutoZero-Remain

In some cases, for example if the P is executing a refresh cycle of the IIC-Bus-programming, it is not useful to start a new AutoZero-action because no new source is selected and an undesired mute would appear at the outputs. For such applications, it can be switched in the AutoZero-Remain-Mode (Bit 6 of the subaddress-byte). If this bit is set to high, the AutoZero will not be invoked and the old adjustment-value remains.

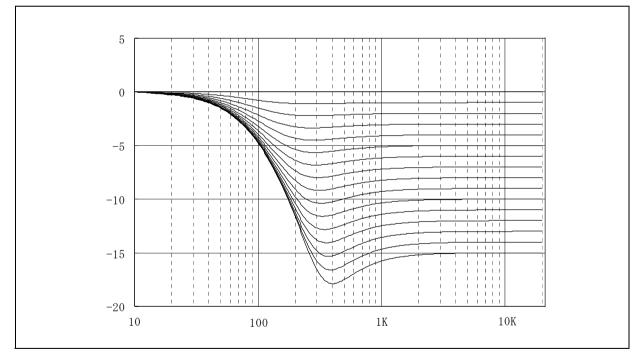
5.3 Loudness

There are four parameters programmable in the loudness stage:

5.3.1 Attenuation

Figure 5 shows the attenuation as a function of frequency at $f_P = 400Hz$

Figure 5. Loudness Attenuation @ f_P = 400Hz.



5.3.2 Peakr Frequency

Figure 6 shows the three possible peak-frequencies 400Hz , 800Hz and 2.4kHz.

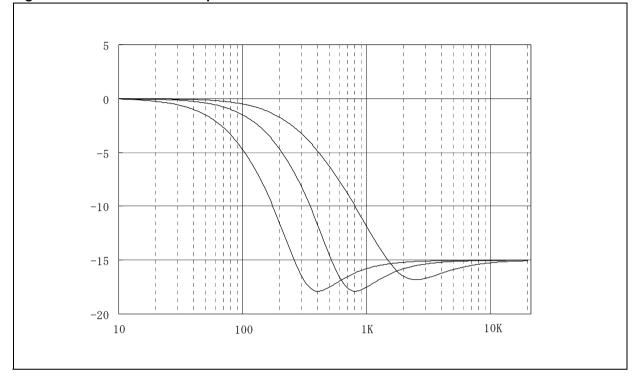
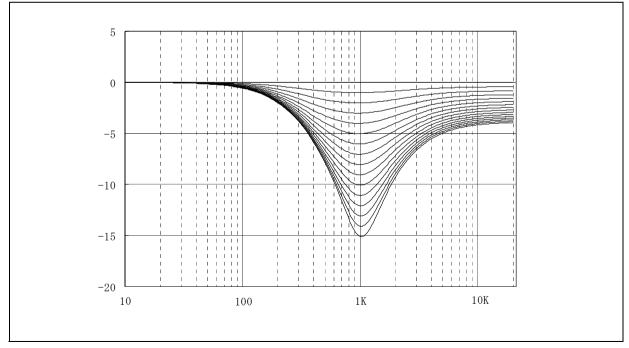


Figure 6. Loudness Center frequencies @ Attn. = 15dB

5.3.3 Low & High Frequency Boost

Figure 7 shows the different Loudness-shapes in low & high frequency boost.

Figure 7. Loudness Attenuation , $f_C = 2.4 KHz$



۲/

5.3.4 Flat Mode

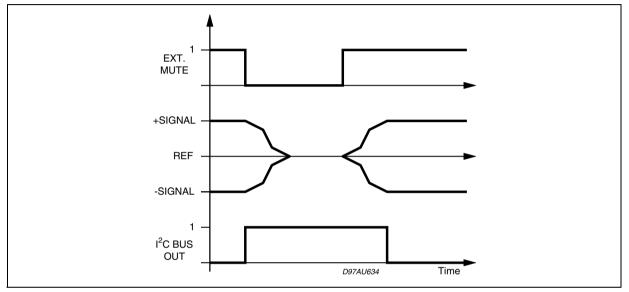
In flat mode the loudness stage works as a 0dB to -15dB attenuator.

5.4 SoftMute

The digitally controlled SoftMute stage allows muting/demuting the signal with a l^2C -bus programmable slope. The mute process can either be activated by the SoftMute pin or by the l^2C -bus. This slope is realized in a special S-shaped curve to mute slow in the critical regions (see Figure 8).

For timing purposes the Bit0 of the I2C-bus output register is set to 1 from the start of muting until the end of demuting.

Figure 8. Sofmute Timing



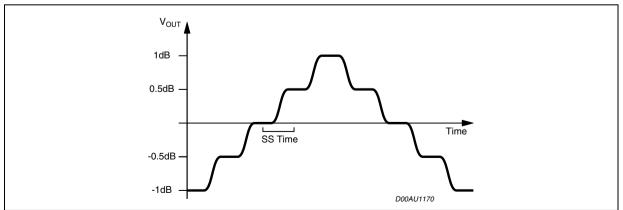
Note: Please notice that a started Mute-action is always terminated and could not be interrupted by a change of the mute -signal

5.5 SoftStep-Volume

When the volume-level is changed audible clicks could appear at the output. The root cause of those clicks

could either be a DC-Offset before the volume-stage or the sudden change of the envelope of the audiosignal. With the SoftStep feature both kinds of clicks could be reduced to a minimum and are no more audible. The blend-time from one step to the next is programmable in four steps.

Figure 9. SoftStep Timing



Note: For steps more than 0.5dB the SoftStep mode should be deactivated because it could generate a hard 1dB step during the blend-time.

5.6 Bass

There are four parameters programmable in the bass stage:

5.6.1 Attenuation

Figure 9 shows the attenuation as a function of frequency at a center frequency of 80Hz.

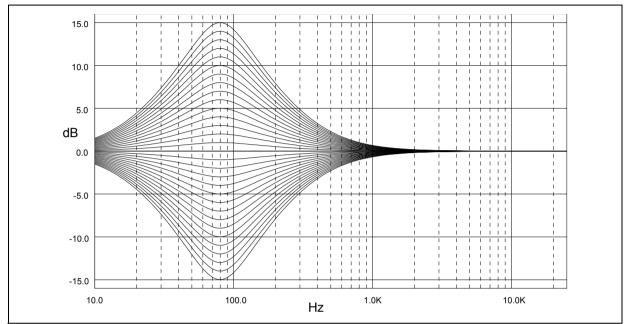
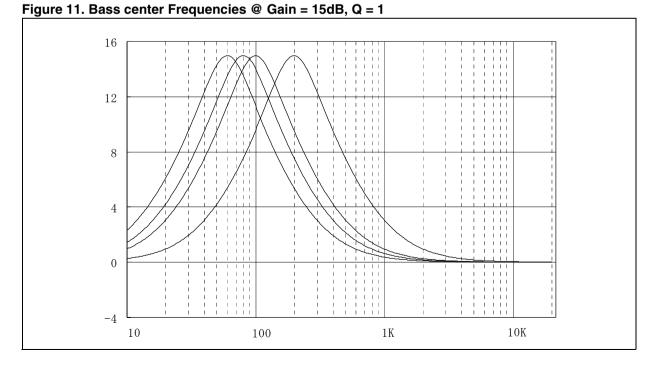


Figure 10. Bass Control @ f_C = 80Hz, Q = 1

5.6.2 Center Frequency

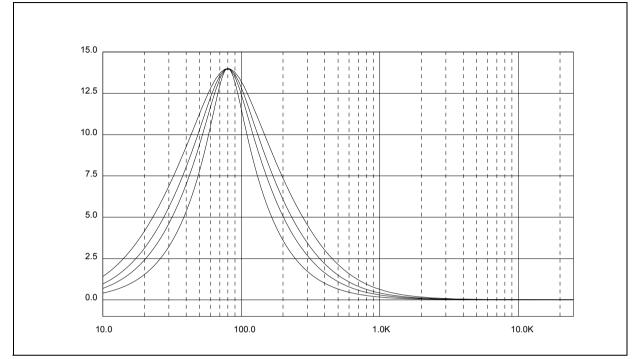
Figure 11 shows the four possible center frequencies 60, 80, 100 and 200Hz.



άγ/

5.6.3 Quality Factors

Figure 12 shows the four possible quality factors 1, 1.25, 1.5 and 2.



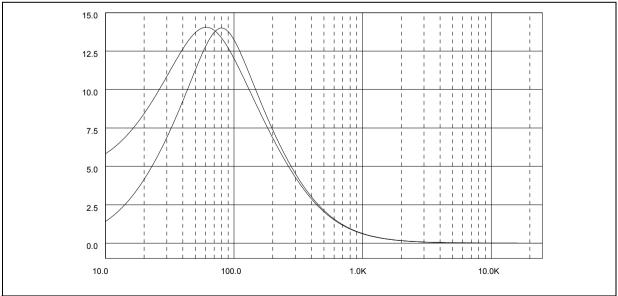


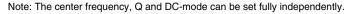
5.6.4 DC Mode

Á7/

It is used for cut only for shelving filter. In this mode the DC-gain is increased by 4.4dB. Inaddition the programmed center frequency and quality factor is decreased by 25% which can be used to reach alternative center frequencies or quality factors.





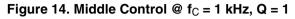


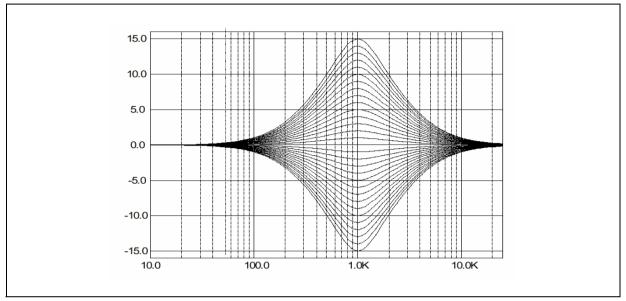
5.7 Middle

There are three parameters programmable in the middle stage:

5.7.1 Attenuation

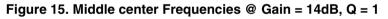
Figure 14 shows the attenuation as a function of frequency at a center frequency of 1kHz.

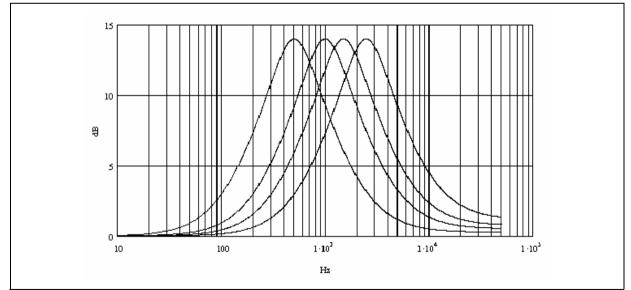




5.7.2 Center Frequency

Figure 14 shows the four possible center frequencies 500Hz, 1kHz, 1.5kHz and 2.5kHz.





άτ/

5.7.3 Quality Factors

Figure 16 shows the four possible quality factors 0.5, 0.75, 1 and 1.25.

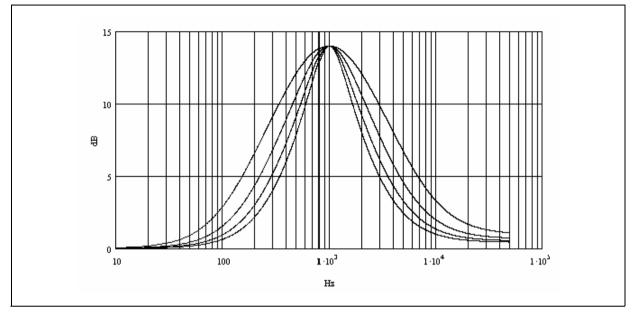


Figure 16. Middle Quality factors @ Gain = 14dB, fc = 1kHz

5.8 Treble

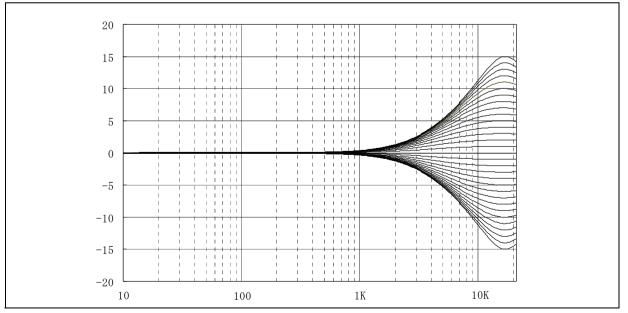
۲۲

There are two parameters programmable in the treble stage:

5.8.1 Attenuation

Figure 16 shows the attenuation as a function of frequency at a center frequency of 17.5kHz.

Figure 17. Treble Control @ f_C = 17.5kHz



5.8.2 Center Frequency

Figure 18 shows the four possible center frequencies 10k, 12.5k, 15k and 17.5kHz.

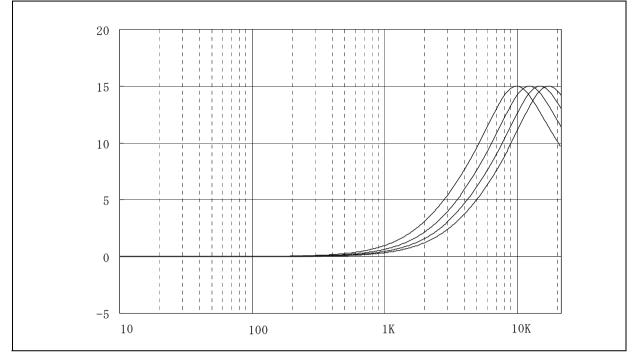
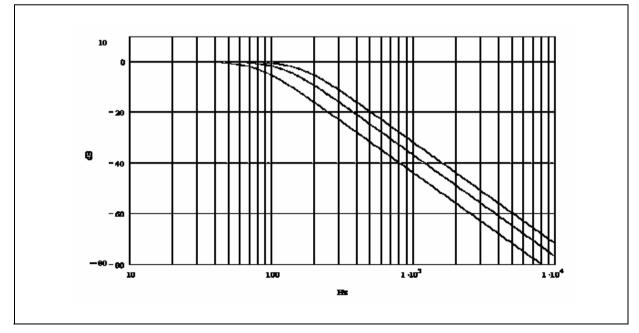


Figure 18. Treble Center Frequencies @ Gain = 15dB

5.9 Subwoofer Filter

The subwoofer lowpass filter has butterworth characteristics with programmable cut-off frequency (80/ 120/160Hz)



۲/

Figure 19. Subwoofer Control

5.10 Spectrum Analyzer

A fully integrated seven-band spectrum analyzer with programmable quality factor is present. The spectrum analyzer consists of seven band pass filters with rectifier and sample capacitor that stores the maximum peak signal level since the last read cycle. This peak signal level can be read by a microprocessor at the SAout-pin. To allow easy interfacing to an analog port of the microprocessor, the output voltage at this pin is referred to device ground.

The microprocessor starts a read cycle with the negative going clock edge at the SAclk input. On the following positive clock edges, the peak signal level for the band pass filters is subsequently switched to SAout. Each analog output data is valid after the time t_{Sadel} . A reset of the sample capacitors is induced whenever SAclk remains high for the time t_{intres} . Note that a proper reset requires the clock signal SAclk to be held at high potential. Figure 20 shows the block diagram and figure 21 illustrates the read cycle timing of the spectrum analyzer.

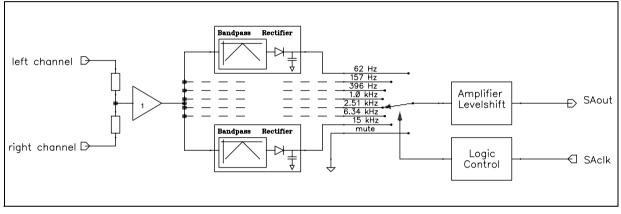
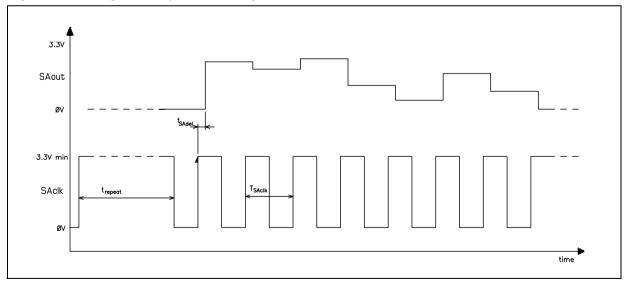


Figure 20. Spectrum analyzer block diagram

Figure 21. Timing of the spectrum analyzer

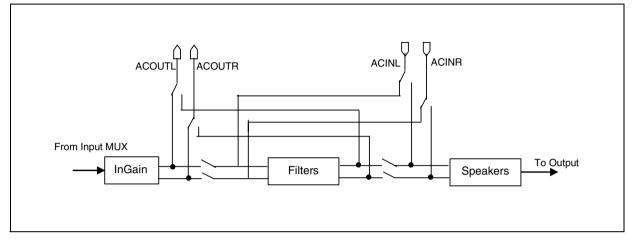
47/



5.11 AC-Coupling

In some applications additional signal manipulations are desired, such as additional band equalizations. For this purpose, an AC-Coupling can be placed before the loudness attenuator or speaker-attenuators, which can be activated or internally shorted by I^2 C-Bus. In short condition, the input-signal of the speaker-attenuator is available at the AC-Outputs. The input-impedance of this AC-Inputs is 50k Ω .

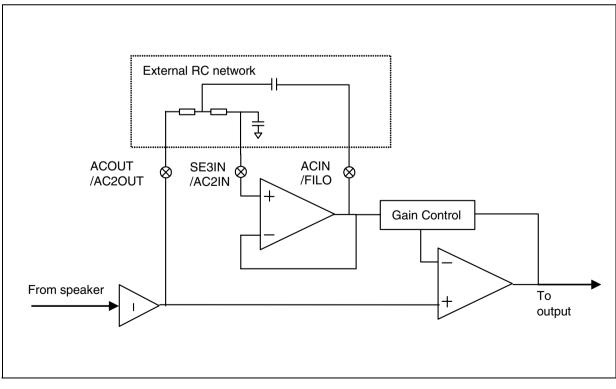




5.12 DSO Applications

For DSO applications, DSO filter is available for additional processing after the speaker control. It is a 2nd order Butterworth highpass filter with selectable flat mode. Figure 23 shows the diagram of the DSO that includes an external RC network.

Figure 23. DSO diagram

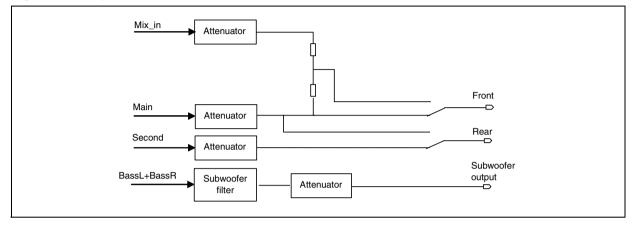


47/

5.13 Output Selector and Mixing

The output-selector allows the front and rear speakers to connect to different sources. The setup of the output selector is shown in Figure 24. A Mixing-stage is placed after the front speaker-attenuator and can be set to mixing-mode. Having a full volume-attenuator for the mix-signal, the stage offers a wide flexibility to adapt the mixing levels.

Figure 24. Output Selector

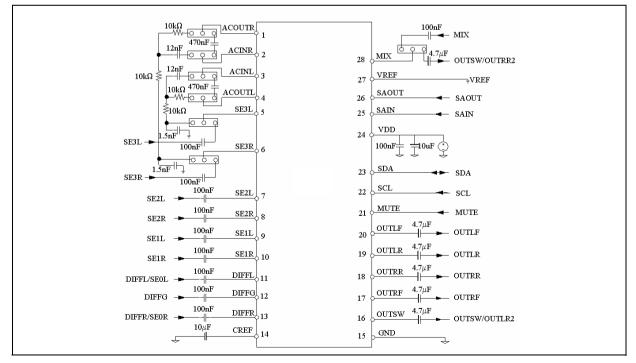


5.14 Audioprocessor Testing

In the test mode, which can be activated by setting bit D7 of the IIC subaddress byte and bit D0 of the testing audioprocessor byte, several internal signals are available at the SE1R pin. In this mode, the input resistance of 100kOhm is disconnected from the pin. Internal signals available for testing are listed in the data-byte specification.

5.15 Test Circuit

Figure 25. Test Circuit



6 I²C BUS SPECIFICATION

6.1 Interface Protocol

The interface protocol comprises:

- a start condition (S)
- a chip address byte (the LSB determines read/write transmission)
- a subaddress byte
- a sequence of data (N-bytes + acknowledge)
- a stop condition (P)
- the max. clock speed is 500kbits/s
- 3.3V logic compatible

6.1.1 Receive Mode

S 1 0 0 1 0 0 R/W ACK TS AZ AI A4 A3 A2 A	1 A0	A1 A0	ACK	DATA	ACK	Ρ
---	------	-------	-----	------	-----	---

S = Start

R/W = "0" -> Receive Mode (Chip can be programmed by μP)

"1" -> Transmission Mode (Data could be received by μP)

ACK = Acknowledge

P = Stop

TS = Testing mode

AZ = Auto zero remain

AI = Auto increment

6.1.2 Transmission Mode

S	1	0	0	0	1	0	0	R/W	ACK	Х	Х	Х	Х	Х	Х	Х	SM	ACK	Ρ

SM = Soft mute activated for main channel

X = Not Used

The transmitted data is automatic updated after each ACK. Transmission can be repeated without new chip address.

6.1.3 Reset Condition

A Power-On-Reset is invoked if the Supply-Voltage is below than 3.5V. After that the following data is written automatically into the registers of all subaddresses:

MSB							LSB
1	1	1	1	1	1	1	0

6.2 Subaddress (receive mode)

Table 7. Subaddress	s (receive mode)
---------------------	------------------

MSB							LSB	FUNCTION
12	11	10	A 4	A3	A2	A1	A0	
0 1								Testing Mode Off On
	0 1							Auto Zero Remain Off On
		0 1						Auto Increment Mode Off On
			0	0	0	0	0	Main Source Selector
			0	0	0	0	1	Main Loudness
			0	0	0	1	0	Soft Mute / Clock Generator
			0	0	0	1	1	Volume
			0	0	1	0	0	Treble
			0	0	1	0	1	Middle
			0	0	1	1	0	Bass
			0	0	1	1	1	Second Source Selector
			0	1	0	0	0	Subwoofer / Middle / Bass
			0	1	0	0	1	Mixing / Gain Effect
			0	1	0	1	0	Speaker Attenuator Left Front
			0	1	0	1	1	Speaker Attenuator Right Front
			0	1	1	0	0	Speaker Attenuator Left Rear
			0	1	1	0	1	Speaker Attenuator Right Rear
			0	1	1	1	0	Mixing Level Control
			0	1	1	1	1	Subwoofer Attenuator
			1	0	0	0	0	Spectrum Analyzer / Clock Source / AC Mode
			1	0	0	0	1	Testing Audio Processor

6.3 Data Byte Specification

Table 8. Main Selector (0)

MSB							LSB	FUNCTION
D7	D6	D5	D4	D3	D2	D1	D0	
								Source Selector
					0	0	0	QD/SE: QD
					0	0	1	SE1
					0	1	0	SE2
					0	1	1	SE3
					1	0	0	QD/SE: SE
					1	0	1	mute
					1	1	х	mute
	0 0 1 1	0 0 1 1	0 0 1 1	0 1 : 0 1				Input Gain OdB 1dB : 14dB 15dB
0 1								Auto Zero on off

Table 9. Main Loudness (1)

MSB							LSB	FUNCTION
D7	D6	D5	D4	D3	D2	D1	D0	
				0 0 : 1 1	0 0 : 1 1	0 0 : 1 1	0 1 : 0 1	Attenuation OdB -1dB : -14dB -15dB
		0 0 1 1	0 1 0 1					Center Frequency Flat 400Hz 800Hz 2400Hz
	0 1							High Boost on off
0 1								Loudness Soft Step on off

57

MSB							LSB	FUNCTION
D7	D6	D5	D4	D3	D2	D1	D0	
							0 1	Soft Mute on off
						0 1		Pin Influence for Mute Pin and IIC IIC
				0 0 1	0 1 x			Soft Mute Time 0.48ms 0.96ms 123ms
	0 0 0 1 1 1 1	0 0 1 0 0 1	0 1 0 1 0 1 0					Soft Step Time 0.160ms 0.321ms 0. 642ms 1.28ms 2.56ms 5.12ms 10.24ms 20.48ms
0 1								Clock Fast Mode on off

Table 10. Soft Mute / Clock Generator (2)

Table 11. Volume / Speaker / Mixing / Subwoofer Attenuation	on (3, 10-15)	
---	---------------	--

MSB							LSB	FUNCTION
D7	D6	D5	D4	D3	D2	D1	D0	
	0 0 0 0 1 1 1	0 0 0 0 0 0 1	0 0 1 1 : 1 1 x	0 0 1 0 0 : 1 1 x	0 0 1 0 0 : 1 1 x	0 0 1 0 0 : 1 1 x	0 1 : 0 1 : 0 1 x	Gain/Attenuation +0dB +1dB : +15dB -0dB -1dB : -78dB -79dB mute
0 1								Soft Step on off

TDA7419

Table 12. Treble Filter (4)

MSB							LSB	FUNCTION
D7	D6	D5	D4	D3	D2	D1	D0	
			0 0 0 1 1 : 1	1 1 0 0 0 0 1 1	1 1 0 0 0 0 1 1	1 1 0 0 0 0 1 1	1 0 1 0 1 : 0 1	Gain/Attenuation -15dB -14dB : -1dB 0dB 0dB +1dB : +14dB +15dB
	0 0 1 1	0 1 0 1						Treble Center Frequency 10.0kHz 12.5kHz 15.0kHz 17.5kHz
0 1								Reference Output Select External Vref (4V) Internal Vref (3.3V)

Table 13. Middle Filter (5)

MSB							LSB	FUNCTION
D7	D6	D5	D4	D3	D2	D1	D0	
			0 0 0 1 1 : 1	1 1 0 0 0 0 1 1	1 1 0 0 0 0 1 1	1 1 0 0 0 0 0 1 1	1 0 1 0 0 1 : 0 1	Gain/Attenuation -15dB -14dB : -1dB 0dB 0dB +1dB : +14dB +15dB
0	0 0 1 1	0 1 0 1						Middle Q Factor 0.5 0.75 1 1.25 Middle Soft Step on off

57

Table 14. Bass Filter (6)

MSB							LSB	FUNCTION
D7	D6	D5	D4	D3	D2	D1	D0	
			0 0 : 0 0	1 1 0 0	1 1 : 0 0	1 1 : 0 0	1 0 : 1 0	Gain/Attenuation -15dB -14dB : -1dB 0dB 0dB
			- 1 - 1 - 1	0 0 1 1	0 0 : 1 1	0 0 : 1 1	0 1 : 0 1	0dB +1dB : +14dB +15dB
	0 0 1	0 1 0 1						Bass Q Factor 1.0 1.25 1.5 2.0
0 1								Bass Soft Step on off

Table 15. Second Source Selector (7)

MSB							LSB	FUNCTION
D7	D6	D5	D4	D3	D2	D1	D0	
								Source Selector
					0	0	0	QD/SE: QD
					0	0	1	SE1
					0	1	0	SE2
					0	1	1	SE3
					1	0	0	QD/SE: SE
					1	0	1	mute
					1	1	х	mute
	0 0 : 1 1	0 0 : 1 1	0 0 1 1	0 1 : 0 1				Input Gain OdB 1dB : 14dB 15dB
0 1								Rear Speaker Source main source second source

Table 16. Subwo	ofer /Middle	/ Bass	(8)
-----------------	--------------	--------	-----

MSB				FUNCTION				
D7	D6	D5	D4	D3	D2	D1	D0	
						0 0 1 1	0 1 0 1	Subwoofer Cut-off Frequency flat 80Hz 120Hz 160Hz
				0 0 1 1	0 1 0 1			Middle Center Frequency 500Hz 1000Hz 1500Hz 2500Hz
		0 0 1 1	0 1 0 1					Bass Center Frequency 60Hz 80Hz 100Hz 200Hz
	0 1							Bass DC Mode on off
0 1								Smoothing Filter on off (bypass)

Table 17. Mixing / Gain Effect (9)

MSB							LSB	FUNCTION
D7	D6	D5	D4	D3	D2	D1	D0	
							0	Mixing to Left Front Speaker on
							1	off
						0 1		Mixing to Right Front Speaker on off
					0 1			Mixing Enable on off
				0 1				Subwoofer Enable (OUTLR2 & OUTRR2) on off
0 0 : 1 1 1 1	0 0 : 0 0 0 1	0 0 : 0 0 1 x	0 1 : 0 1 x x x					Gain Effect for DSO Filter 4dB 6dB : 20dB 22dB 0dB 0dB

57

MSB							LSB	FUNCTION
D7	D6	D5	D4	D3	D2	D1	D0	
							0	Spectrum Analyzer Filter Q Factor 3.5 1.75
						0 1		Reset Mode IIC Auto
					0 1			Spectrum Analyzer Source Bass InGain
				0 1				Spectrum Analyzer Run on off
			0 1					Reset on off
		0 1						Clock Source internal external
0 0 1 1	0 1 0 1							Coupling Mode DC Coupling (without DSO) AC coupling after InGain DC Coupling (with DSO) AC coupling after Bass

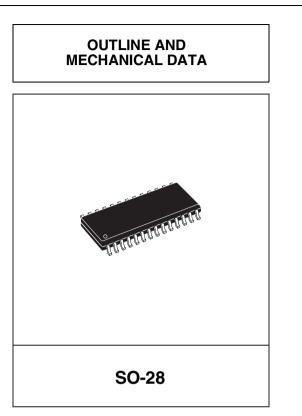
Table 18. Spectrum Analyzer / Clock Source / AC Mode (16)

Table 19. Testing Audio Processor (17)

MSB							LSB	FUNCTION
D7	D6	D5	D4	D3	D2	D1	D0	
								Audio Processor Testing Mode
							0	off
							1	on
								Test Multiplexer
		0	0	0	0	0		Left InGain
		0	0	0	0	1		Left InGain
		0	0	0	1	0		Left Loudness
		0	0	0	1	1		Left Loudness
		0	0	1	0	0		Left Volume
		0	0	1	0	1		Left Volume
		0	0	1	1	0		Left Treble
		0	0	1	1	1		Left Treble
		0	1	0	0	0		Left Middle
		0	1	0	0	1		SMCLK
		0	1	0	1	0		Left Bass
		0	1	0	1	1		VrefSCR
		0	1	1	0	0		VGB1.26
		0	1	1	0	1		SSCLK
		0	1	1	1	0		Clock200
		0	1	1	1	1		Mon
		1	0	0	0	х		Ref5V5
		1	0	0	1	х		BPout<1>
		1	0	1	0	х		BPout<2>
		1	0	1	1	х		BPout<3>
		1	1	0	0	х		BPout<4>
		1	1	0	1	х		BPout<5>
		1	1	1	0	х		BPout<6>
		1	1	1	1	х		BPout<7>
х	х							Not used

Figure 26. SO-28 Mechanical Data & Package Dimensions

DIM.		mm		inch			
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
А			2.65			0.104	
a1	0.1		0.3	0.004		0.012	
b	0.35		0.49	0.014		0.019	
b1	0.23		0.32	0.009		0.013	
С		0.5			0.020		
c1	45° (typ.)						
D	17.7		18.1	0.697		0.713	
Е	10		10.65	0.394		0.419	
е		1.27			0.050		
e3		16.51			0.65		
F	7.4		7.6	0.291		0.299	
L	0.4		1.27	0.016		0.050	
S			8 ° (n	nax.)			



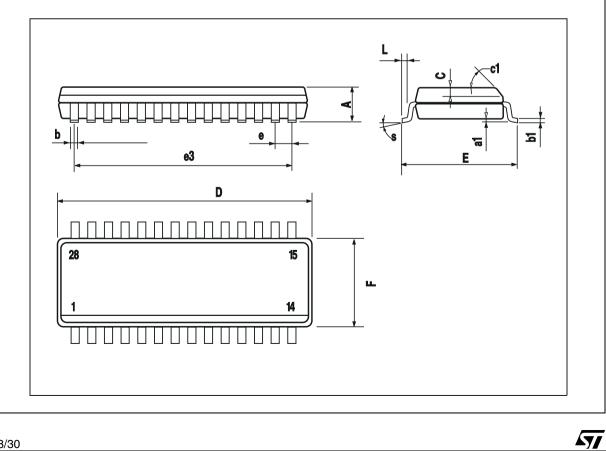


Table 20. Revision History

Date	Revision	Description of Changes
November 2004	1	First Issue
March 2005	2	Inserted new values in Electrical Characteristics

Information furnished is believed to be accurate and reliable. However, STMicroelectronics assumes no responsibility for the consequences of use of such information nor for any infringement of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of STMicroelectronics. Specifications mentioned in this publication are subject to change without notice. This publication supersedes and replaces all information previously supplied. STMicroelectronics products are not authorized for use as critical components in life support devices or systems without express written approval of STMicroelectronics.

The ST logo is a registered trademark of STMicroelectronics. All other names are the property of their respective owners

© 2005 STMicroelectronics - All rights reserved

STMicroelectronics group of companies

Australia - Belgium - Brazil - Canada - China - Czech Republic - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan -Malaysia - Malta - Morocco - Singapore - Spain - Sweden - Switzerland - United Kingdom - United States of America www.st.com